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Basic design of MOSFET, four-phase, digital integrated circuits

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BASIC DESIGN OF MOSFET, FOUR-PHASE, DIGITAL INTEGRATED CIRCUITS

By

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A

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Abstract

MOSFET is defined as metal oxide semiconductor field-effect transistor. The integrated circuit design relates strictly to logic and switching circuits rather than linear circuits.

The design of MOS circuits is primarily one of charge and discharge of stray capacitance through MOSFETS used as switches and active loads. To better take advantage of the possibilities of MOS technology, four-phase (4ϕ) circuitry is developed. It offers higher speeds and lower power while permitting higher circuit density than does static or two-phase (2ϕ) logic.

Equations are developed that apply directly to the design of four-phase logic along with examples of circuitry that show their use. The most unique of these is the equation for discharge through two or more MOSFETS in series from a saturated condition. The effects of stray capacitance on circuit performance are explained. Methods for overcoming deleterious effects and taking advantage of helpful effects are discussed and solved. The main effect is that of discharge of the stored charge on a logic node through the gate to source overlap capacitance when a phase clock returns to ground.

In all, a complete method for designing 4ϕ circuitry is developed and explained in appropriate examples.

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Introduction

MOSFET, metal oxide semiconductor field-effect transistor, integrated circuit technology has not existed long enough to have a wealth of circuit design technology available to anyone that might wish to become acquainted with the practices of industry. In fact, the practices of industry itself are not clearly presented or available to most persons desiring information. Only a scattered few articles on circuit design are available in the literature and these are usually very superficial due to the limited background of most readers. Most MOSFET literature has been in the area of processing and single device physics, stabilization of the oxide surface states and mobility.

The purpose of this thesis is to develop a state-of-the-art design procedure for four-phase (4ϕ) circuits which are currently only beginning to appear on the commercial market. Enough background and supplementary material is supplied to enable most readers with a rudimentary knowledge of MOSFET technology to understand the design procedures without constantly referring to outside papers.

The MOSFET circuit design book, MOSFET in Circuit Design by Robert H. Crawford, will be used as a source for all equations used in this thesis.[1] "MOSFET" will generally be shortened to "MOS".

Although MOS design technology is very scarce, no attempt will be made to reiterate the sum of all design rules. Only the background necessary for an understanding of the very special area which is developed is presented. Device fabrication and processing integrated circuits are usually the secrets of a particular commercial enterprise and are explained only as necessary to the understanding of the parameters used in the design of a circuit.

Review of the Literature

Only a very few papers have been published on 4ϕ design. There have been a number published utilizing 2ϕ design or general design.[2,3]

A basic article on 4ϕ design and comparison to 2ϕ design, by Karp and de Atley, gives the basic beginnings of MOS logic design and elementary switching theory.[4] It is a good paper for basic equations and overall theory, but oversimplification leads to errors in their design procedures. A notable example of this is their statement that there is no need for the devices in an inverter to be different sizes in a 4ϕ MOS system. Most of their conclusions are correct, but the amount of area saved and speed increase are exaggerated. One circuit is given, a J-K Flip-Flop, to illustrate 4ϕ MOS circuitry, but several errors in either design or printing will keep the circuit from ever operating. They also state that time for discharge, or turn on time, is determined by the single calculation in the saturated region. This is only a rough approximation. It must also include the time spent discharging in the triode region.

One of the best reports on MOS Technology is the research report published by the Air Force Avionic Laboratory.[5] The research was performed by the Microelectronics Division of Philco-Ford Corporation. All circuit development in this report must be carefully considered by the individual user. At best, the report gives a good starting point, but the results derived are characteristic of the initial assumptions and present very narrow results especially in the realm of 4ϕ MOS design equations.

There are two books dealing mainly with MOS technology.[1,6] The book by Crawford is generally a more circuits oriented approach and is a

general reference for this paper. The other by Richman is mainly a device oriented book and has excellent background material on theory of operation.

For earlier work on MOS devices and structures, the reader is referred to papers by H. K. J. Ihantola[7] and C. T. Sah[8]. Most all important and pertinent references other than these are thoroughly referenced in the two previously described books and in most cases are listed by both.

Chapter II

Background of MOS Fabrication and Parameters

This chapter deals with the rudiments of basic MOS fabrication only as background to help explain their operation and not as a help for actual device production.

The equations and relationships presented are taken from Crawford (Reference I) and are not proven. Others have derived equations governing the operation of the MOSFET and have come up with similar results. The differences mainly being slight additions that make the equations more nearly exact curve fits of the characteristic curves, but which do not make significant contributions to the actual practical design of integrated circuits.

Fabrication

The MOSFET has a basic construction in integrated circuits as shown. P-channel enhancement MOSFETS are generally used because they are easiest to fabricate. The reason lies in the ease of consistent reproduction of the threshold voltage V_T. Threshold voltage may be expressed as

$$V_T = - (Q_{SS} + Q_D)/C \quad [1]$$

where

Q_{SS} = effective surface-state charge density per unit area

Q_D = bulk charge per unit area associated with the channel depletion region

C = capacitance of the gate to channel per unit area.

The bulk charge Q_D is positive for P-channel MOSFETS and negative for N-channel MOSFETS. For typical MOSFET starting material, 4-5 ohm-cm substrate resistivity, the Q_{SS} and Q_D terms are approximately equal. This means that very good process control is required to maintain a constant V_T with N-channel MOSFETS, since Q_{SS} and Q_D subtract in the equation for V_T. However, in P-channel MOSFETS the terms add, making P-channel MOSFETS much easier to fabricate with a relatively constant threshold voltage. By use of a lower substrate resistivity starting material, 1-2 ohm-cm, N-channel MOSFETS may be made with some reproducibility. High back gate bias effects make them unacceptable for MOS circuit design.

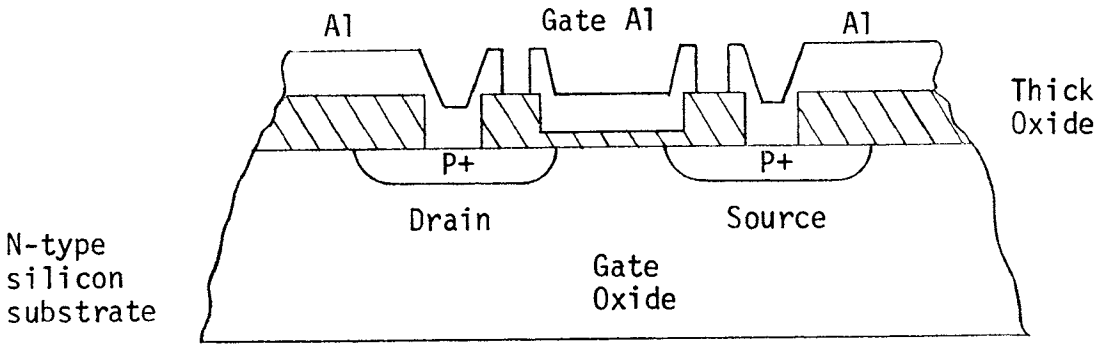
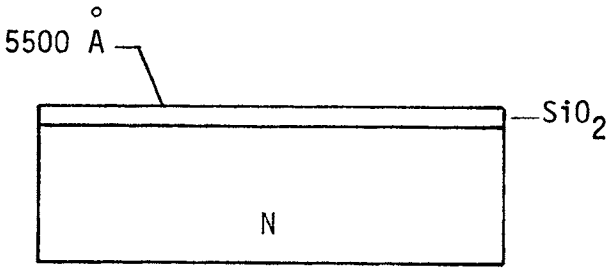


Figure 1

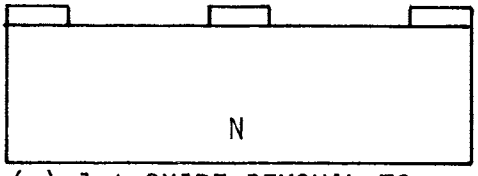
Cross Section of a MOSFET

The above figure is used for illustration only and is not drawn to scale. The following dimensions show typical MOSFET size.

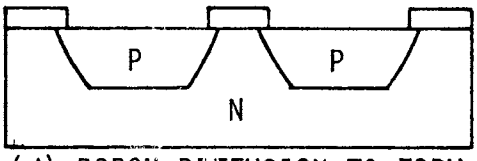
(a) STARTING MATERIAL



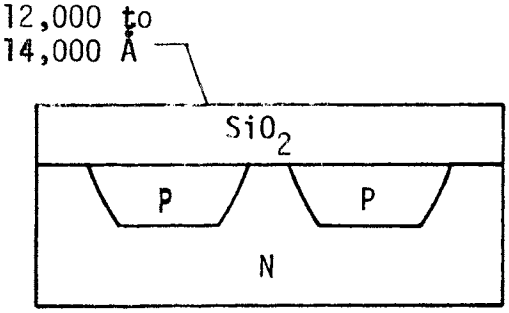
(b) GROW DIFFUSION OXIDE MASK



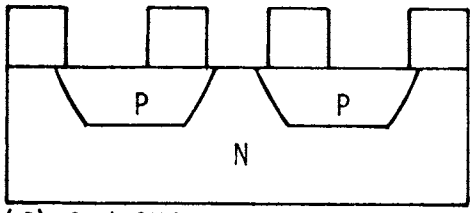
(c) 1st OXIDE REMOVAL TO EXPOSE DIFFUSED AREAS



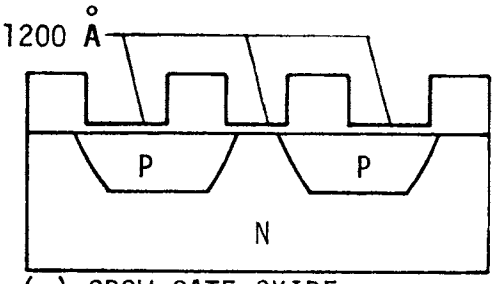
(d) BORON DIFFUSION TO FORM DRAIN-SOURCE REGIONS



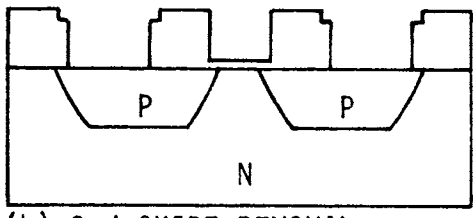
(e) GROW THICK OXIDE



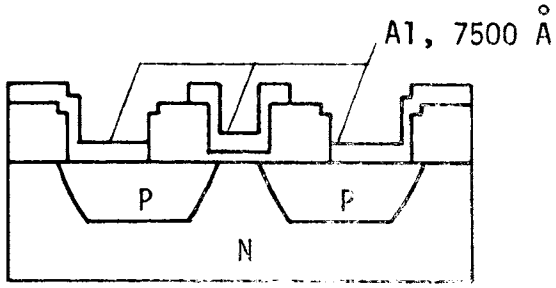
(f) 2nd OXIDE REMOVAL TO EXPOSE THE GATE AND CONTACT REGIONS



(g) GROW GATE OXIDE



(h) 3rd OXIDE REMOVAL CONTACT REGIONS



(i) ALUMINUM METALLIZATION

Figure 2

MOSFET Fabrication Technique

Source and drain

P+ Diffusions
Depth = 2200 Å
Width = 0.3 mil min

Gate Oxide
Depth = 1000 Å
Width = 0.3 mil min

Al
Depth = 7000 Å
Width = 0.4 mil min

Slice Thickness

Thick Oxide = 10,000 Å

Substrate Resistivity 2-6 Ω cm

Diffusion Sheet Resistance = 50-150 Ω/□

Table 1

Typical MOSFET Dimensions

Operation

This is approximately the standard fabrication used throughout industry now for what is termed as a thick oxide process. The operation is as follows for the above structure, a P-channel enhancement mode transistor. The gate, including the gate oxide and the gate metal, controls the charge in the channel, where the channel is the substrate surface between the source and drain. As a negative voltage is applied to the gate, free electrons in the N-type silicon are repelled until the surface is essentially depleted. Then a further increase in the gate bias attracts positive holes to the surface finally inverting the channel from N-type to P-type material.

If a voltage is applied between drain and source, a current will flow from the drain to the source across the P-channel. The inverted layer extends all the way across the channel for low values of drain voltage and, therefore, the current is determined by the gate voltage and the

drain voltage. However, for a constant gate voltage the drain current finally becomes saturated with increasing drain voltage. The drain current produces an IR drop that opposes the field produced by the gate such that an inversion layer may no longer be formed. Under these conditions, the channel "pinches off" and the current saturates at this level, essentially independent of the drain voltage. The pinch-off voltage is a very important parameter in designing MOS circuits and will be called the threshold voltage and labeled V_T.

Characteristic curves of the previous situation follow:

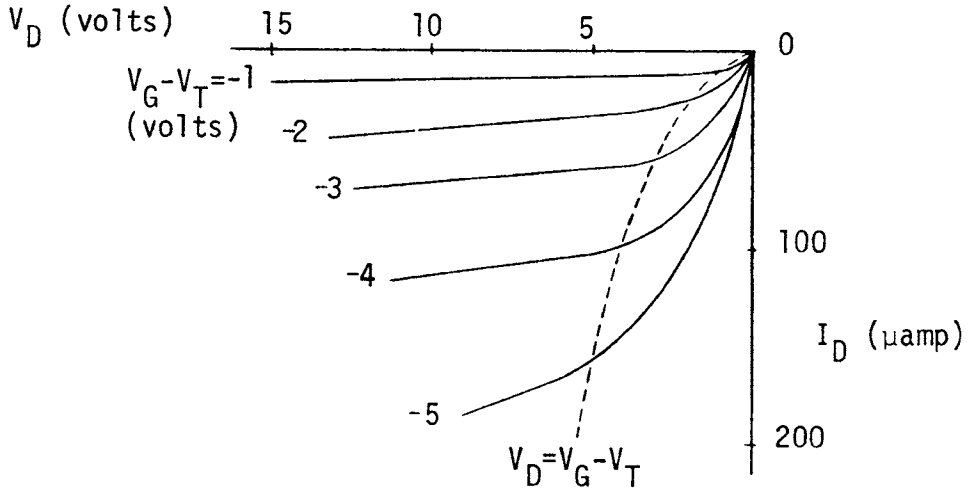


Figure 3a

Characteristic Curve of a Typical P-Channel MOSFET

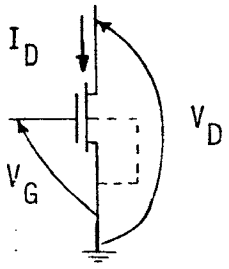


Figure 3b

Reference for Characteristics in 3a

Equations and Relationships

Standard equations relating these characteristics are separated into two regions. The first region called the triode region defines the curve before saturation and is the area in which drain current is determined by both gate and drain voltages. The second region is the saturation region and is the area in which drain current is determined only by gate voltage. The separation of the two regions is given by the equation:

$$V_D = V_G - V_T$$

Greater gate voltages force entry into the triode region while an increase in drain voltage causes saturation to be reached. The drain current in the triode region is given by[1]

$$I_D = + \beta \left[(V_G - V_T) V_D - 1/2 V_D^2 \right] \qquad 1.$$

In the saturation region, the drain current is given by

$$I_D = + \beta/2 (V_G - V_T)^2 \qquad 2.$$

In both of these equations

$$\beta = \frac{W}{L} \frac{\varepsilon_{ox} \mu_p}{t_{ox}} \qquad 3.$$

Where W/L is the width to length ratio of the channel oxide, ε_{ox} is the permittivity of the gate oxide, μ_p is the mobility of the minority carriers (holes) in the silicon, and is the thickness of the gate oxide.

I_D is drain current.

V_G is the gate bias with respect to the source.

V_D is the drain bias with respect to the source.

V_T is the threshold or pinch-off voltage with source and substrate connected.

These two equations for drain current will form the basis for the 4ϕ design to be developed.

One other parameter that will be useful is the transconductance and is defined as

$$gm = \frac{\partial I_D}{\partial V_G} \Bigg|_{V_D} \qquad 4.$$

Differentiating the equation for the current in the saturation region yields

$$gm = \frac{\partial I_D}{\partial V_G} \Bigg|_{V_D} = \beta (V_G - V_T) \qquad 5.$$

Notice that the transconductance may be increased in two ways. The first is by increasing the value of voltage V_G. The second is by increasing the value of β which, as can be seen by equation 3, is proportional to W/L or the width to length ratio of the transistor. In practice, both of these are varied to give the desired result. The size of the MOSFET, however, is the single most important variable in design and may vary widely within a single integrated circuit. Unlike discrete design where a designer may have only a few size devices available, the MOS designer has at his command almost any size device he wishes excluding those too small to process and those so large that the area consumed is prohibitive.

Chapter III

Basic Design Theory

MOS integrated circuits are made possible only by the improved technology of silicon preparation and diffused transistors. These circuits are pursued because of their simple construction and LSI (large scale integration) possibilities. Miniaturization is now the key word to success in all electronic fields and especially logic fields. Users are demanding more and more functions in less space with each succeeding request.

Presently the majority of MOS design work is being done in the logic fields since MOS enhancement mode transistors are ideally suited for boolean logic. They have a definite logic '1' voltage below which they will not operate, and the logic zero level is well suited to be the ground level available in MOS logic.

MOS integrated circuits have a number of advantages besides their adaptability to boolean algebra. The process for forming the circuits involves relatively few steps and thus improves the overall yield from a slice of silicon. The simplicity of the circuits, utilizing only MOS devices either as transistors or as active loads makes possible a very high device density such as 250 transistors in a 2500 mil^2 area, including connections, to make a working circuit. An area this size can be formed by a chip .05 x .05 inches.

The one major disadvantage of MOS circuits at the present time is their speed. Experimental circuits may go to 10 MHz but most circuits are in the 500 KHZ to 2 MHz range, not a very impressive figure compared to bipolar integrated circuits.

The MOS as a device is inherently fast. However, the manner in which they are incorporated into circuit layouts decreases the operating speed of the circuit tremendously. The main factor in this slowness is stray capacitance. This capacitance along with its direct effects determine the following reasons for slow MOS circuits from a competitive standpoint:

1) Stray capacitance loading the outputs.
2) Overlap of coupling capacitances decreasing logic levels.
3) Speed vs. size.
4) Speed vs. power dissipation.

It is for these reasons that 4ϕ logic among other types of special MOS logic is being developed. Four-phase is a way to get faster circuits with very little additional effort.

Four-phase logic utilizes four clocks to switch a circuit instead of the usual two. Previous types of circuit design, 2ϕ and D-C circuits, will be explained and developed as a background for 4ϕ operation.

Two-Phase and D-C Operation

Assume the configuration of Figure 4 for a simple D-C logic inverter. All voltages are taken with respect to the substrate which is grounded. In Figure 4 there are two transistors, Q1 is the load and Q2 is the driver. Q1 in this case is a saturated load since the drain and gate are at the same potential, where saturation was defined as $V_D \geq V_G - V_T$. The lower device transfers the input data to the output. When IN is '0' Q2 is off and $V_{out} = (V_{DD} - V_T)$ which will be called the logic '1' level. Now when IN is at the '1' level, usually the same magnitude as V_{out}, Q2 is on, and most of the voltage will be dropped across the load Q1. The

slight amount of voltage across Q2 will be termed the logic '0' level. Now we have the configuration giving a '0' output when the input is '1' and giving a '1' output when there is a '0' input.

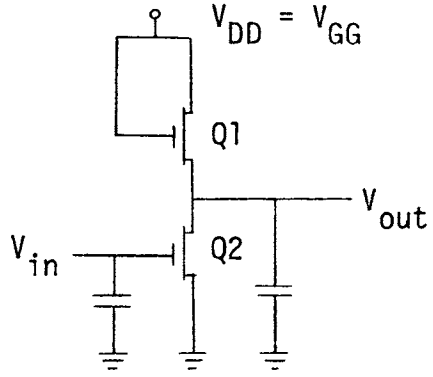


Figure 4
D-C Logic Inverter

The two capacitors shown are stray capacitances of the circuit and are always present. They are useful and yet detrimental at the same time, which will be explained shortly. The driver device is generally made with a W/L ratio 20 times as large as the load to get acceptable logic levels.

As the output capacitance charges during an input level of zero, the gate to source voltage V_{GS} becomes increasingly smaller until finally the load transistor is shut off.

$$V_G - V_T \leq V_{out}$$

In the saturation region the current expression as given before was

$$I_D = \frac{\beta}{2} \quad (V_G - V_T)^2$$

Current through the capacitor C_L is

$$i = \frac{C\ d(V_{out})}{dt}$$

Therefore,

$$\frac{C\ dV_{out}}{dt} = (\beta/2)(V_G - V_{out} - V_T)^2$$

or

$$d(V_{out}) = (\beta/2C)[(V_G - V_T)^2 - 2(V_G - V_T)\ V_{out} + V_{out}^2]\ dt$$

Let $V_1 = V_G - V_T$

$$\int_o^V \frac{d(V_{out})}{(\beta/2C)(V_1 - V_{out})^2} = \int_o^t dt$$

Let $X^2 = (V_1 - V_{out})^2$

$$\int_o^{V_1 - X} \frac{dx}{(\beta/2C)(X^2)} = \int_o^t dt$$

$$t = (2C/\beta)\left[\frac{1}{V_1 - V_{out}} - \frac{1}{V_1}\right]$$

Let $\tau = \dfrac{C}{\beta(V_G - V_T)}$

Substituting for V_1 and collecting terms for τ,

$$V_{out} = V_1 \frac{t/\tau}{2+ t/\tau} \qquad 6.$$

By this formula the speed of the capacitor charge from 10% to 90% is 17.78τ

$$t_{0\text{-}90\%} - t_{0\text{-}10\%} = 18\tau - .22\tau = 17.78\tau \qquad 7.$$

The value will be given by 18τ from here on, being the value from 0 to 90%. Now suppose that after C_L has been charged, V_{DD} is turned off and V_{in} becomes a '1'. Now we have the following condition:

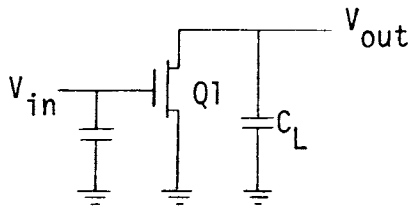


Figure 5
Driver Discharge

The capacitor will now discharge through Q2 and the device will be first in the saturated region and then as V_{out} decreases, it will enter the triode region.

V_{out} (initial) = V_{in}

Saturation $V_{out} \geq V_{in} - V_T$

Triode $V_{out} \leq V_{in} - V_T$

To make the above circuit a two-phase circuit, we have only to add phase lines to the load gates.

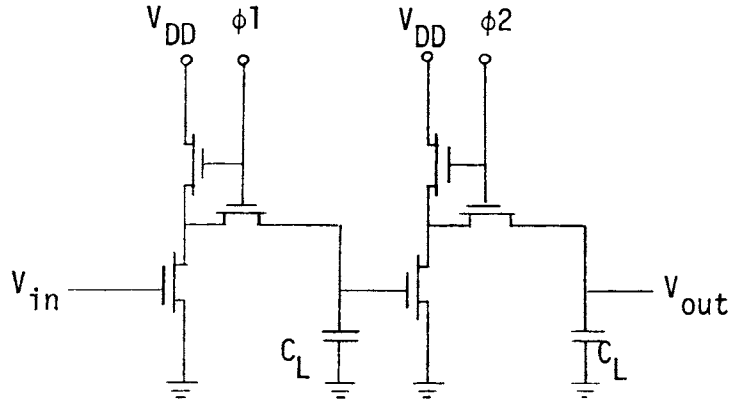


Figure 6a
2ϕ Dynamic Bit

V_G is now a clocked phase voltage. Note that there are now two individual inverters; both turned on by different phase clocks, $\phi 1$ and $\phi 2$. The total of these two inverters comprises a simple storage bit of a shift register. A typical timing diagram would look like the following:

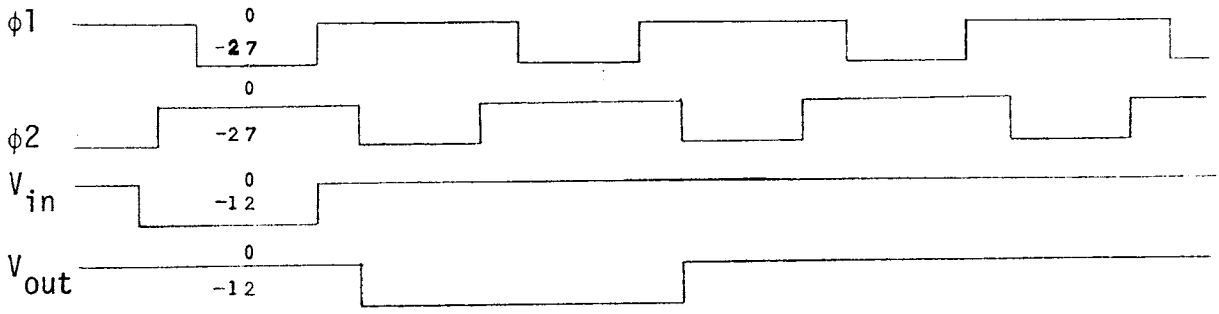


Figure 6b
Timing Sequence for Figure 5a

The output cannot change state until $\phi 2$ either lets C_L charge or discharge depending on the previous state of the output of the first stage.

The main operating principle of a two-phase circuit is to charge and discharge the stray capacitive load by a voltage divider action. The input formation is clocked through the first inverter during $\phi 1$ and through

the second inverter during $\phi 2$. The output need be true only after $\phi 2$ goes off since it may still be changing states during $\phi 2$. Since it is separated from the last stage inverter after $\phi 2$ goes off, the output may be read anytime during $\phi 1$ and the dead time between $\phi 1$ and $\phi 2$.

The voltage divider action of a two-phase circuit has a number of disadvantages. The output capacitance has to be charged to a voltage below the threshold voltage V_T when the input is a logical '1'. This generally means that for a favorable noise level the driver device must be about 20 times as big as the load device as may be determined by setting the load current equal to the driver current. When the output is charged to a high level during a logical zero input, the output capacitance and the load size determine the speed of charging. For very fast speeds, the driver device becomes exhorbitantly large and defeats the purpose of MOS LSI. Two-phase circuits also provide a D-C path to ground which means a relatively high power consumption. So, the three main disadvantages are power requirements, slow speed, and size.

Four Phase Circuitry and Operation

To overcome these disadvantages, 4ϕ circuits are being introduced. A circuit diagram of one configuration of a 4ϕ circuit is shown in Figure 7 and is the type circuit that will be developed here. Other configurations that may be used are shown in Figure 9. The circuits in Figure 7 and Figure 9 all have advantages and disadvantages over each other. Most all of them have three advantages over 2ϕ circuits: (1) They generally may be designed for higher speeds; (2) They use less power since there will be no dc path to ground; (3) They do not work on the voltage divider principle and therefore are smaller.

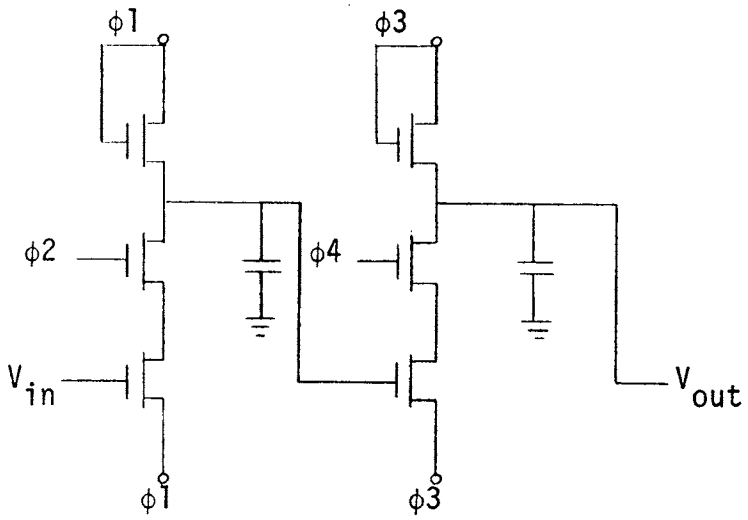
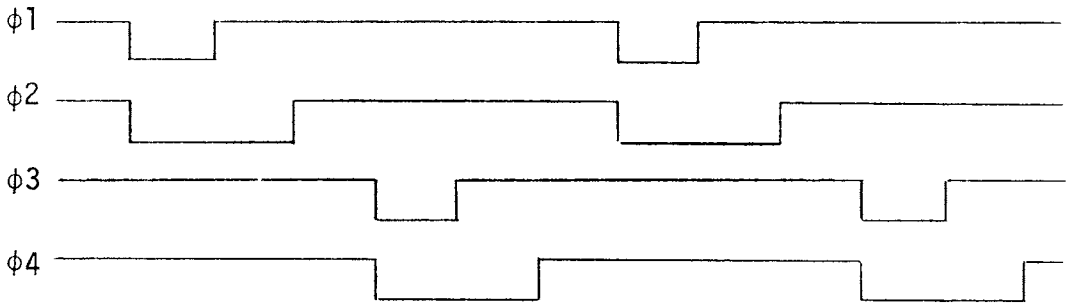


Figure 7
Basic 4φ Bit

I



II

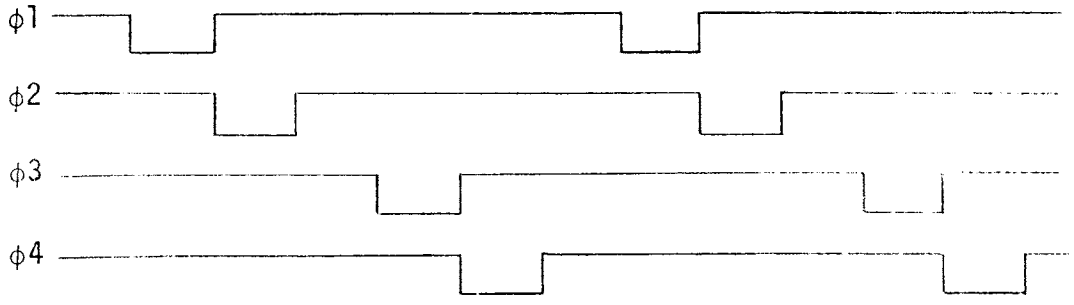


Figure 8
4φ Timing Sequence

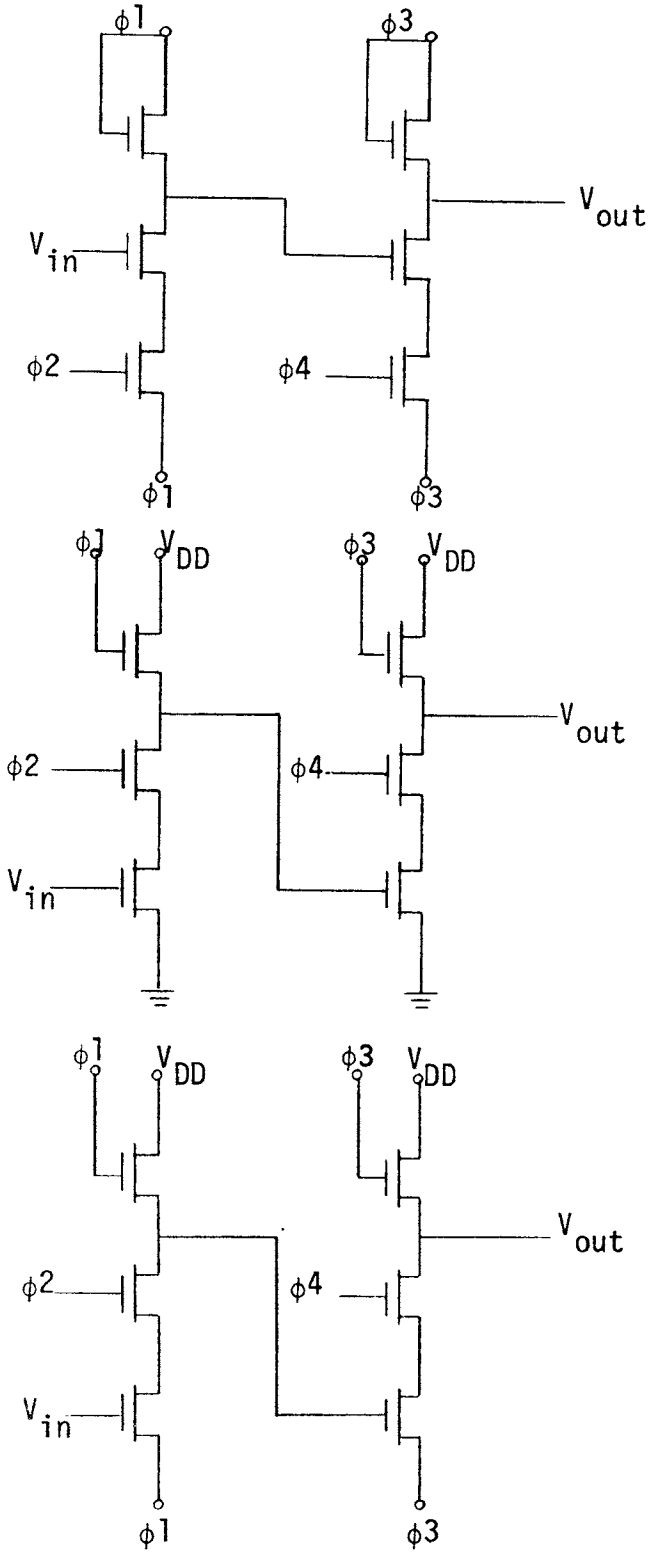


Figure 9

Basic 4φ Configurations

Although the three circuit diagrams in Figure 9 are very similar, the design and physical layouts may be radically different. Also their clocking schemes may be very different depending on the demands of the designer and the situation.

The clocking system of the circuit in Figure 7 may be either of two types (Figure 8). These timing diagrams are different in that $\phi 1$ and $\phi 2$ overlap, and $\phi 3$ and $\phi 4$ overlap in the first sequence whereas they are separate in the second sequence. In some cases, it may be preferred that the phases are all of the same time duration. In the first sequence, this would mean that the duration of $\phi 2$ after $\phi 1$, would be the same length as $\phi 1$.

There are advantages to both schemes of clocking depending on customer needs, availability of generators, and power requirements. It should be said that power in a four-phase circuit is all A-C power and is directly proportional to the frequency of operation.

$$P = C\, V_{DD}\, V_{out}\, f \qquad 8.$$

where C is the capacitance of all the gates to which a ϕ supplies voltage, V_{DD} is the voltage of the phase line, V_{out} is the output level, and f is the frequency of operation.

In this design development, the circuits will be of the form of Figure 7 or 9 and the clocking system will be of the form of Figure 8, sequence I.

Giving the diagram of Figure 7 in detail will also show a few more stray capacitances.

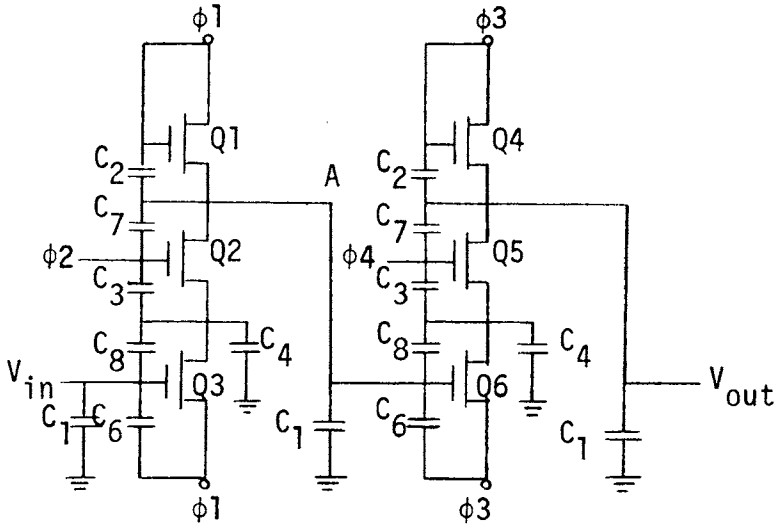


Figure 10
4φ Bit Showing Stray Capacitance

Operation of a four-phase circuit will now be given. The input signal V_{in} precedes or occurs during φ2, clock time. Clock φ1, and φ2 at logic '1' levels are said to be "on". Phases 1 and 2 turn on at the same time. When φ1, φ2, φ3, φ4 are not on, they are at the ground level logical '0' and are used as such.

Phase one turns on and charges C_1 and C_4, the main one of these being C_1. Both of these capacitors are charged only because φ1, and φ2 are on at the same time. When φ1 turns on and charges C_1, φ2 turns on Q2 which lets φ1 also charge C_4. This is an important aspect of overlapping clocks. Now when φ1 goes off and φ2 is still on, the input level of V_{in} determines whether C_1, stage 1, will charge or discharge. If V_{in} is a logical '1' then Q3 is also on, and C_1 and C_4 discharge through Q2 and Q3 to ground which is the off state of φ1. When φ2 turns off φ3 comes on and charges C_1, stage 2. Phase three turns off, φ4 stays on, and since C_1, stage 1, has discharged, Q6 is off, and C_1, stage 2, stays charged

to the previous level. If V_{in} had been a logical '0', C_1 stage 1, would have remained charged during $\phi 2$ and Q6 would have been turned on. With this condition, C_1, stage 2, would have discharged during $\phi 4$ and the output level would be '0'.

The 4ϕ bit just described has a logical output of the same level as the input. The signal in has been delayed by one cycle, however, and a string of these bits may be used as a delay line. The same series of bits may also be used as a shift register or as a storage register. With modifications, it may have any combination of serial in, parallel in, serial out, parallel out operation of information read and write.

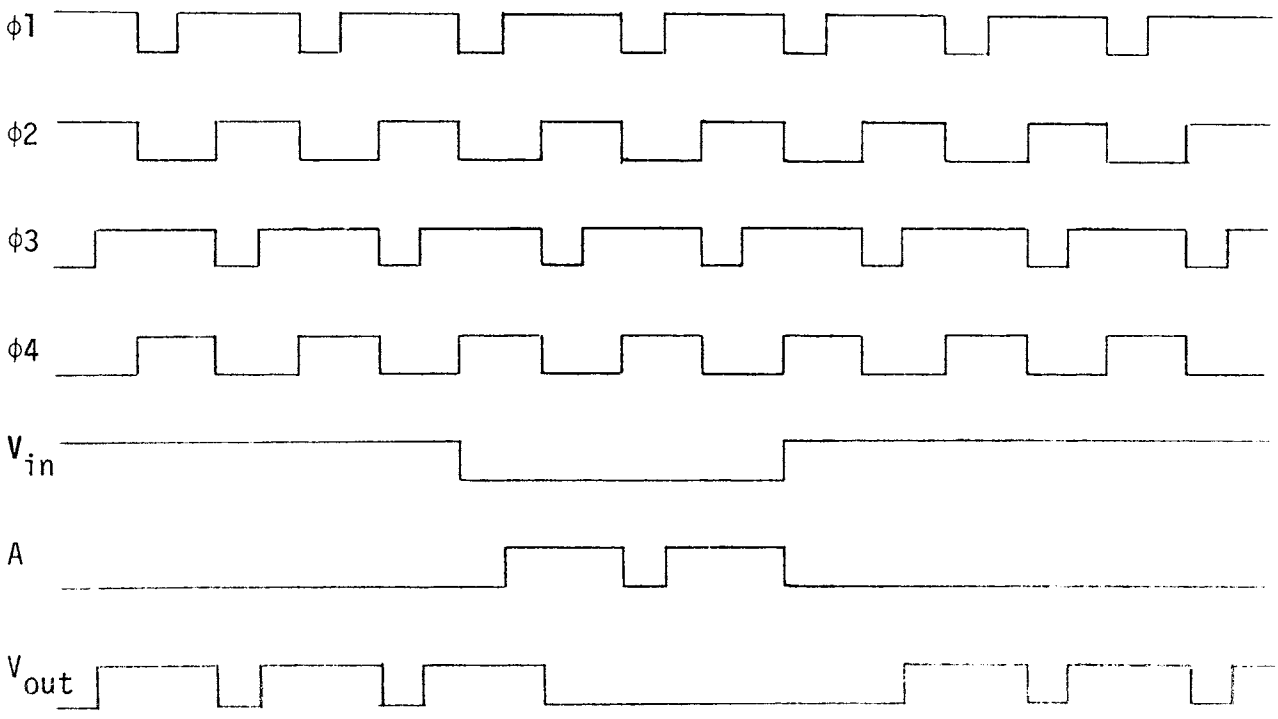


Figure 11
Timing Sequence of Figure 10

The first stage of this shift register bit is of prime importance in the design. The basic inverter is the building block of all 4ϕ circuits and therefore must be analyzed carefully. The first inverter stage of Figure 10 will form the basis for this study.

Capacitance charge and discharge comprises the total sum of MOS circuit design including 4ϕ design. The inverter charge and discharge of C_1 comprises the major portion of the design. The rest of the capacitors are included in the design only if they affect this concept. The overlapping clocks serve to eliminate a major problem arising out of the stray capacitance.

Assume that $\phi 2$ did not turn on until after $\phi 1$ had turned off. Q2 is off until $\phi 2$ comes on. The precharged level of C_1 will now have to charge the stray capacitance C_4 if V_{in} is at the zero level. This will decrease the output level of V_{out} according to the following:

$$Q_T = C_1 V_{out}$$

$$V_{C_1} \text{ (final)} = \frac{C_1 V_{out}}{C_1 + C_4}$$

Due to physical layout of an integrated circuit, C_4 has a minimum attainable lower limit. Now if an output of 10 volts is the precharged level of V_{out}, then C_1 must be made at least 9 times larger than C_4 to insure a drop in output level of no more than 1 volt.

$$V_{out} \text{ (final)} = \left(V_{out}\right)\frac{9\ C_4}{9\ C_4 + C_4} = 9/10\ V_{out} \text{ (initial)}$$

Added capacitance has two disadvantages. It is added by increasing the diffused lead size between Q1 and Q2 which also increases the leakage current, and added capacitance causes a decrease in the speed of the inverter which may only be overcome by increasing the size of the devices which also adds more capacitance to C_4. Only by very excellent circuit layout under special conditions may C_4 be made a minimum value.

However, with overlapping clocks, C_4 is charged through Q2 by $\phi 1$, and there is no problem with the output level dropping due to the capacitance division of the voltage.

Another problem that might arise due to the overlapping clocks, however, is a false turn on of Q3. The same mechanism that charges C_4 also charges C_8 and C_1 of Q3. Since these capacitances are in series, the charge will distribute equally between them, and there will be a voltage division of V_{C4} such that

$$V_{C6} = \frac{V_{C4}\ C_1}{C_1 + C_6} \qquad V_{C1} = \frac{V_{C4}\ C_6}{C_1 + C_6}$$

C_1 in this case is analogous to C_1 of the output and is a fairly large capacitance relative to C_6. C_6 is a very small overlap capacitance. C_6 may be a value around .016 pf while C_1 is probably about .20 pf or greater. The ratio now turns out to be

$$V_1 = V_{C4}\ \frac{.016}{.016 + .20} = .074\ V_{\phi 1}$$

Now the highest voltage in the circuit $V_{\phi 1}$ will not exceed -27V, so -27V

will be used as the worst case for V_{C4}. Assume also that $V_T = -4V$.

$$V_{C1} = -(.074)\ (27)V$$

$$= -2.0 > V_T = -4V$$

There is no chance of falsely turning Q3 on since the magnitude of the threshold voltage V_T would have to be exceeded.

The sizes of the capacitances in the above analysis are determined by the layout on the semiconductor chip. Therefore, good layout decreases all the capacitances, yet still maintains the proper relative capacitance sizes. A working analysis of capacitance is given later in Chapter 3. As said before, when non-overlapping clocks are used, C_4 must be made very small in comparison to C_1 to avoid a serious drop in the output voltage level. An acceptable ratio may usually only be made by increasing C_1 after C_4 is made as small as possible in a design. This, however, slows the circuit down appreciably or necessitates the use of larger transistors. Another solution to the problem is to insert a "pull-up" capacitor between the gate of Q2 and the source of Q2 as shown in Figure 12.

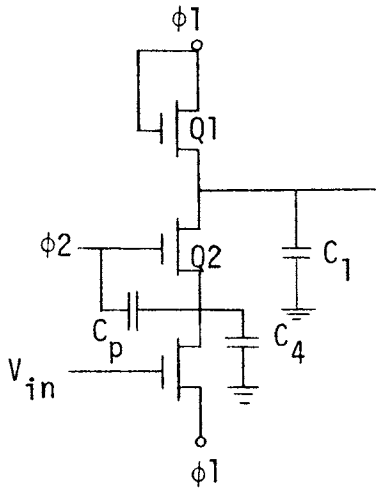


Figure 12

4ϕ Inverter Showing Added Pull-up Capacitor C_p

The pull-up capacitor is relatively easy to incorporate in the circuit and just entails a large thin-oxide overlap on the P region of the source which is covered by $\phi 2$.

With this circuit configuration, $\phi 2$ will help charge C_4 and thus lessen the voltage drop of V_{out}. The voltage division is

$$V_{C4} = V_{\phi 2} \frac{C_p}{C_4 + C_p}$$

Thus, the larger C_p is made, the higher the voltage level that C_4 could attain from $\phi 2$. The circuit layout for Figure 12 is shown in Figure 13.

The only drawbacks are increased area for the layout and added capacitance for the $\phi 2$ clock to drive at the required speed. A very thorough analysis of this type of design is included in the Philco-Ford research report No. 5.[5]

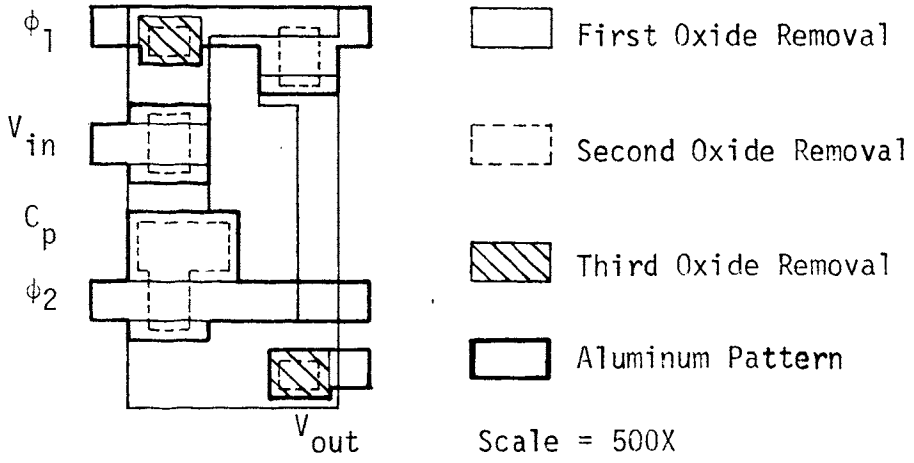


Figure 13

Inverter Showing
Inclusion of
Pull-up Capacitor

Chapter IV

Transistor Size Theory

With the above background, the theory of charge and discharge of a load capacitance will begin. In MOS logic design charge and discharge of capacitive loads and coupling capacitance determine the operation of the entire circuit.

Capacitance along with transistor size determine the speed of operation, power dissipated, and logic levels within the circuit. The amount of capacitance and its distribution affect transistor size. The sizes of the transistors determine the charge and discharge times of the capacitance. This chapter deals with determination of the proper size transistors to produce a circuit that will operate at the desired frequency.

Charge of the Load

Since 4ϕ circuits operate on two sets of identical clocks ϕ1, ϕ2 and ϕ3, ϕ4, in a symmetrical manner, all circuit calculations applying to one set also applies to the other set. Figure 14 shows operation from one set of clocks.

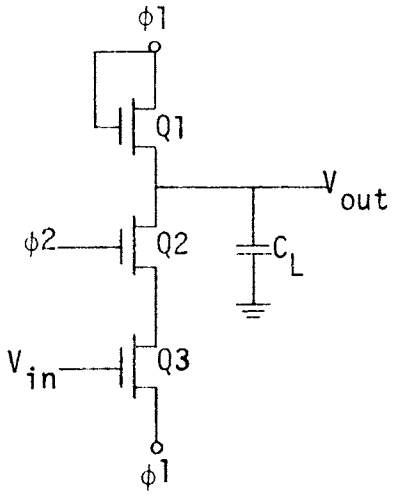


Figure 14
4ϕ Dynamic Operation

The operation of the circuit in Figure 14 involves only the charge and discharge of the load capacitor C_L. The load transistor Q1 charges C_L to a predetermined voltage level, and then when $\phi 1$ returns to the ground state, this voltage either stays constant or discharges, depending on the V_{in} value.

The circuit for charging C_L is shown in Figure 15.

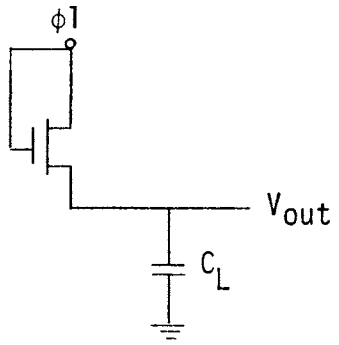


Figure 15
Charge of the Load Capacitance

As was shown in Chapter III the charge time of this configuration from the 10% to 90% points is given by

$$t_{10\text{-}90\%} = 17.78\tau$$

$$\tau = \frac{C}{gm} = \frac{C}{(V_G - V_T)}$$

Therefore, to determine the proper size MOSFET to charge a given load to its 90% voltage level β is given by

$$\beta = \frac{18C}{t\,(V_G - V_T)} \text{ mhos/volt}$$

β may be made larger than this if a safety factor is needed for the charge time. If, however, the output voltage is not to be allowed to go to its maximum voltage, then the original equation (eq. 6) must be used.

$$V_{out}(t) = V_{max} \frac{t/\tau}{2 + t/\tau} \qquad 9.$$

or,

$$\tau = t(V_{max} - V_{out})/(2\ V_{out})$$

also

$$\tau = \frac{C}{gm} = \frac{C}{\beta(V_G - V_T)}$$

$$\beta = \frac{C}{(V_G - V_T)}$$

$$\frac{1}{\tau} = \frac{2\ V_{out}}{t(V_{max} - V_{out})} \qquad 10.$$

$$\beta = \frac{2C\ V_{out}}{t(V_{max} - V_{out})(V_G - V_T)} \qquad 11.$$

This equation for β must be used to determine the desired value of V_{out}. In this case after β has been calculated, the minimum value of C and the minimum value of V_T that are possible are used to refigure $V_{out(max)}$. The value of the highest output voltage possible is needed to figure the discharge time when the data input is true. Herein lies the most difficult part of the 4ϕ design -- the discharge of the load capacitance.

Discharge of the Load

Discharge: By One Transistor

First discharge through one transistor is considered and secondly with two transistors in series. Figure 5 shows discharge through one transistor.

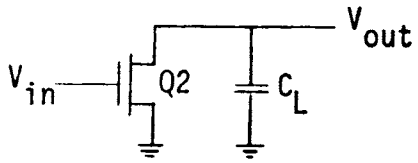


Figure 5
Driver Discharge

The discharge time of V_{out} through Q2 depends on β or MOSFET size and the magnitudes of V_{in}, V_{out} and C_2. Depending on the magnitudes of V_{out} and V_{in}, the MOSFET will be in either the triode region or the saturated region. The most time-consuming case will be that of a MOSFET in the saturated region, considering that V_{out} is the same in both cases. In this case, the device will follow a discharge path as shown in Figure 16.

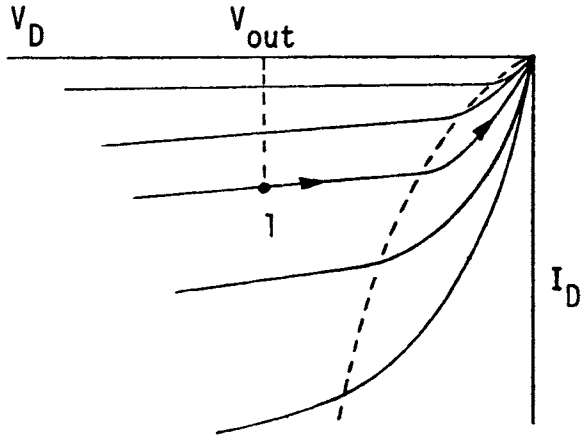


Figure 16
Characteristic Curve Showing Discharge Path

The discharge would start at Point 1 in the saturated region and follow the I=constant line until V_{out} drops so low that $V_{out} < V_G - V_T$. Then the discharge would be in the triode region for the remainder of the time.

Discharge in the saturated region with a constant current is given by:

$$t = \frac{C\Delta V}{I} = \frac{C\Delta V}{(\beta/2)(V_G - V_T)^2} \qquad 12.$$

where C is the capacitance, $\beta/2\ (V_G - V_T)^2$ is the constant current, and ΔV is the amount of the voltage drop to get into the triode region. Since $V_D \leq V_G - V_T$ for the triode region or $V_{out} \leq V_G - V_T$, then $\Delta V = V_{out}\ (max) - (V_G - V_T)$.

After the MOSFET enters the triode region, the equations differ since there is no longer a constant current source. In this region,

$$C \frac{dV_{out}}{dt} = \beta(V_G - V_T)V_{out} - (\beta/2)\, V^2$$

$$d\, V_{out} = \left[\frac{\beta}{C}\,(V_G - V_T)V_{out} - \frac{\beta}{2C}\, V_{out}^2\right] \quad dt$$

$$\int \frac{dV_{out}}{(V_G - V_T)V_{out} - 1/2\ V_{out}^2} = (\beta/C) \int dt$$

$$\frac{1}{(V_G - V_T} \ln \left[\frac{(V_G - V_T) - 1/2\ V_{out}}{V_{out}}\right] + K = [\beta/C]\ t$$

at $t = 0$, $V_G - V_T = V_{out}$

therefore $$K = \frac{\ln 2}{V_G - V_T}$$

$$\frac{C}{\beta(V_G - V_T)} \ln\left[\frac{2(V_G - V_T) - V_{out}}{V_{out}}\right] = t$$

$$V_{out} = \frac{2V_1}{e^{(t/\tau)}+1} = \frac{2V_1 e^{-(t/\tau)}}{e^{-(t/\tau)}+1} \qquad 13.$$

Using this equation, the time required to go from 100% to 10% of the initial voltage may be figured.

$$\begin{aligned} &100\% \text{ to } 10\% \quad t = (\ln 19)\tau = 2.94\tau \\ &100\% \text{ to } 90\% \quad t = (\ln 1.22)\tau = .20\tau \qquad 14. \\ &t_{90\% \text{ to } 10\%} = 2.94\tau - .20\tau = 2.74\tau \end{aligned}$$

Now the equation for the discharge 90% to 10% will be given by:

$$t_D = \underbrace{\frac{2\,C\Delta V}{\beta(V_G - V_T)^2}}_{\text{Saturation period}} + \underbrace{\frac{2.94\,C}{\beta(V_G - V_T)}}_{\text{Triode period}} \qquad 15.$$

Series Discharge

The next case of discharge is the discharge through two MOSFETS in series.

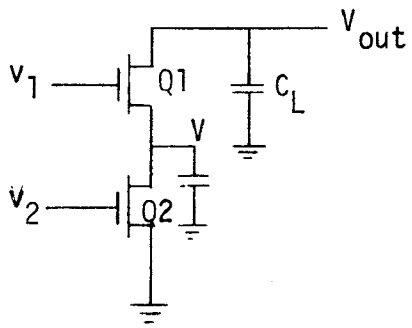


Figure 17
Series Discharge

There are four cases possible in the discharge of this configuration.

1) Q1 saturated, Q2 saturated
2) Q1 saturated, Q2 unsaturated
3) Q1 unsaturated, Q2 saturated
4) Q1 unsaturated, Q2 unsaturated

All of these cases are dependent on the voltage levels of the inputs and the voltage level of the output. The first, second, and third cases always revert to the fourth case in the latter stages of discharge.

The cases stated mathematically are given by

Case 1 $V > (v_2 - V_T)$ $(V_{out} - V) > (v_1 - V - V_T)$
Case 2 $V < (v_2 - V_T)$ $(V_{out} - V) > (v_1 - V - V_T)$
Case 3 $V > (v_2 - V_T)$ $(V_{out} - V) < (v_1 - V - V_T)$
Case 4 $V < (v_2 - V_T)$ $(V_{out} - V) < (v_1 - V - V_T)$ (16)

The voltages in these equations are defined by Figure 17.
As an example, the first of these will be evaluated with respect to optimization. From this a conclusion will be drawn. The other three,

due to the complexity of their solutions and the value of the results, will not be optimized. Instead, a more valuable aspect of design will be discussed in Chapter V. The first case follows.

Case 1 Q_1 saturated, Q_2 saturated $V > (V_2 - V_T)$,

$$(V_{out} - V) > (V_1 - V - V_T)$$

Let $(v_2 - V_{T2}) = V_2$ and $(v_1 - V_{T1}) = V_1$

$$I_{QI} = I_{Q2} \quad , \quad I = -(\beta/2)\,(V_G - V_T)^2$$

$$I_{\beta 1} = -(\beta_1/2)\,(V_1 - V)^2$$

$$I_{\beta 2} = -(\beta_2/2)\,(V_2)^2$$

$$(\beta_1/2)\,(V_1 - V)^2 = (\beta_2/2)\,(V_2)^2$$

$$\beta_1\,(V_1^2 - 2V_1\,V + V^2) = \beta_2\,V_2^2$$

Let

$$\beta_2/\beta_1 = y \qquad V_1/V_2 = x$$

$$V^2 - 2VV_1 + V_1^2 - y\,V_2^2 = 0$$

$$V = \frac{2V_1}{2} \pm \sqrt{\frac{4V_1^2 - 4(V_1^2 - y\,V_2^2)}{2}} = V_1 \pm \sqrt{y}\,V_2 = V_2\,(x \pm \sqrt{y})$$

Under this requirement for V, both MOSFETS will be in saturation. The output voltage as a function of time as given by both the top and bottom MOSFET is:

$$V_{out} = (\beta_2/C)(V_2^2\,t) = (\beta_1/C)(V_1 - V)^2\,t \qquad 17.$$

or time is given by:

$$t = \frac{V_{out}\, C}{\beta_2\, V_2^2} = \frac{V_{out}\, C}{\beta_1\, (V_1 - V)^2} \qquad 18.$$

The time will be fastest when V is as small as possible. Therefore, V is found as a function of X and Y.

$$V = V_2\, (X - \sqrt{Y})$$

$$\text{Minimum when } X = \sqrt{Y}$$

In the other case when $V = V_2\, (X + \sqrt{Y})$ the only minimum solution is to make one or both the gate voltages equal to zero. This solution prevents any discharge of the voltage output at all and is clearly not a practical solution.

Therefore, in the saturated - saturated case, minimum discharge time should take place when $X = \sqrt{Y}$. The results of laboratory investigation show that the maximum speed of discharge is obtained for most cases under the following conditions,

$$\frac{V_1}{V_2} = \frac{\beta_2}{\beta_1}$$

where $\beta_1 + \beta_2 = \text{constant}$ and $V_1 = v_{g1} - V_{T1}$, $V_2 = v_{g2} - V_{T2}$

The exact solutions for the optimization of the other three cases would certainly be interesting but at this point not worth the effort. Each case puts severe restrictions on the voltage levels within a circuit which cannot be strictly followed due to stray capacitive coupling. Also, the results of such an investigation and design cannot be monitored within

an actual circuit for three important reasons:

1. Circuit size
2. Only metallized points may be probed
3. Capacitance associated with probe apparatus can be as much as 100 times more than internal node capacitance.

Therefore, only under laboratory breadboard test conditions can the situation be approximated. Under these conditions the above result relating input gate voltages and MOSFET sizes was determined. This result will be used in all following design examples. After determination of MOSFET sizes, the design concludes with a thorough analysis of capacitive effects of the actual circuit layout.

Determination of Device Size Example

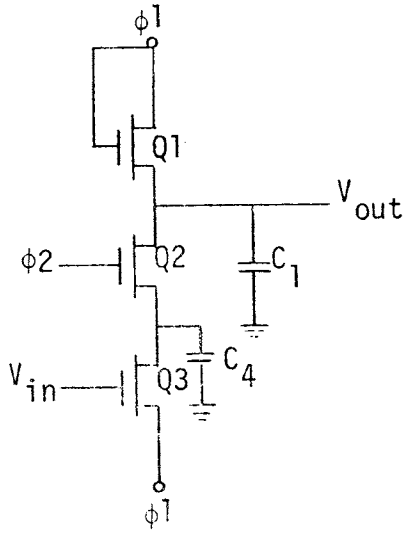


Figure 18
4φ Inverter

The operation of the inverter in Figure 18 has been previously described. MOSFET Q1 charges C_1 during $\phi 1$ time. This time is predetermined by the desired rate of operation which will here be assumed to be 5 MHz. This makes $\phi 1$ 50 nsec and $\phi 2$ 100 nsec. MOSFET Q1 is a saturated device and will charge C_2 according to equation (6).

$$V = \frac{V_1 \; t/\tau}{2 + t/\tau} \qquad 6.$$

The maximum voltage obtainable, V_1, is $V_{\phi 1} - V_T$. To charge to the maximum V_1 takes theoretically an infinite amount of time. Since the charge time doubles from 80% to 90% of the maximum voltage, it will be desirable to only charge to 80% of the maximum voltage.

Assume $V_{\phi 1} = -27V$, $V_{T1} = -7V$, therefore $V_1 = -20V$

$$(80\%)\ (V_1) = -16V$$

Equation 11 gives equation 6 solved for β

$$\beta = \frac{2C\ V_{out}}{t(V_{max} - V_{out})(V_G - V_T)} \qquad 19.$$

C_1 will be assumed to be 0.25 pf. Solving for β

$$\beta = \frac{2(.25X10^{-12})(16)}{(50X10^{-9})(20-16)(27-7)}$$

$$\beta = 2X10^{-6}\ \text{mho/v}$$

Next assume a '1' level V_{in} signal. C_1 will discharge during $\phi 2$ after $\phi 1$ turns off. The discharge time for C_1 is given by equation 15

for one MOSFET.

$$t_D = \frac{2C \quad V}{\beta(V_G - V_G)^2} + \frac{2.94C}{\beta(+V_G - V_T)} \qquad 20.$$

To expand this equation to cover more than one MOSFET in series, a summation is used.

$$t_D = \sum_{i=1}^{N} \left[\frac{2C \quad V_i}{\beta_i (V_G - V_T)_i^2} + \frac{2.94C}{\beta_i (V_G - V_T)_i} \right] \qquad 21.$$

For two MOSFETS as in our case

$$t_D = \frac{2C \triangle V_1}{\beta_1 (V_G - V_T)_1^2} + \frac{2.94C}{\beta_1 (V_G - V_T)_1} + \frac{2C \triangle V_2}{\beta_2 (V_G - V_T)_2^2} + \frac{2.94C}{\beta_2 (V_G - V_T)} \qquad 22.$$

This equation now simulates the time in the saturated region plus the time spent in the non-linear triode region by two MOSFETS in series having a combined resistance. The equation has been laboratory tested and found to agree almost exactly with calculated values when two MOSFETS are used. When more than two MOSFETS are used, the calculated time gradually becomes greater than the measured time for discharge. In this instance, six MOSFETS in series discharged 10% faster than the time calculated for them. When using discrete components, the β for each device must be measured at the approximate operating conditions of the circuit, and these values are used in the equation.

The following voltage levels are the maximum values that may be obtained under steady state conditions:

$$V_{out} = V_{\phi 1} - V_{T1} \qquad V_{C1} = V_{out} - V_{T2}$$

The following example illustrates the discharge of C_1 during $\phi 2$ using equation 22:

Initial conditions and assumptions

t_D = 50 nsec

C = 0.25 pf $\qquad V_{out}$ = -16 volts

V_{C1} = -16 + 6.5 = -9.5 volts

V_{T1} = -7.0 volts
V_{T2} = -6.5 volts
V_{T3} = -5.0 volts
} 1

$V_{G1} = V_{\phi 2}$ = -16 volts $\qquad \Delta V_1$ = -6.5 volts

$V_{G2} = V_{in}$ = -16 volts $\qquad \Delta V_2$ = 0 volts

Solving equation 22,

$$50X10^{-9} = 1/\beta_2 \quad \frac{(.25X10^{-12})}{(16-6.5)} \quad \frac{2(6.5)}{(16-6.5)} + 2.94 \quad + 1/\beta_3 \frac{(.25X10^{-12})}{(16-6.5)} \quad 2.94$$

$$50X10^{-9} = \frac{.113X10^{-12}}{\beta_2} + \frac{.077X10^{-12}}{\beta_3}$$

$$\frac{V_2}{V_3} = \frac{\beta_3}{\beta_2}, \quad \frac{V_2}{V_3} = \frac{16-6.5}{16-5.0}$$

Solving these two equations for β_3 in terms of β_2,

$$\beta_3 = .85\beta_2$$

Due to the incremental sizes in which MOSFETS must be made, the final size of MOSFET 2 will be the same as MOSFET 3, so let $\beta_2 = \beta_3$. The equation is easily solved either way.

$$\beta_2 = 3.8 \times 10^{-6} \text{ mhos/volt}$$

The β's for the load and the inverters have now been determined.

$$\beta_1 = 2.0X10^{-6} \text{ mhos/volt}$$

$$\beta_2 = \beta_3 = 3.8X10^{-6} \text{ mhos/volt}$$

The actual size of the device is related to β by

$$\frac{W}{L} = \frac{\beta}{\beta'}, \quad \beta' = \frac{t_{ox}}{\varepsilon_{ox}\mu_p}$$

$$t_{ox} = 1000\text{Å}$$

$$\varepsilon_{ox} = 35.4X10^{-14} \text{ f/cm}$$

$$\mu_p = 140 \text{ cm}^2\text{/volt-sec at } 100°C$$

$$\beta' = 5X10^{-6} \text{ mhos/volt}$$

$$\left(\frac{W}{L}\right)_1 = 2.0/5.0 = 0.4$$

$$\left(\frac{W}{L}\right)_{2,3} = 3.8/5.0 \approx 0.8$$

The physically smallest size MOSFET possible to build has a W/L ratio of 1.5, which is a MOSFET with dimensions of W = 3 mil, L = 2 mil. Processing requirements prohibit dimensions smaller than these. Therefore, the minimum size MOSFET will be used in this example since it exceeds the calculated requirements. The values just given describe a normal internal inverter or one-half shift register bit.

Chapter V

Effects of Capacitance on Circuit Operation

Earlier in Chapter III a short discussion was given on the effects of stray capacitance with and without the benefit of overlapping clocks. It was shown that a logic one level can be degraded due to charge sharing between the capacitors in an inverter. The overall problem of retaining the proper voltage levels in a circuit is a very complex one involving all possible stray capacitance in a circuit. The capacitance itself changes magnitude with voltage levels either as a reverse biased p-n junction or as the length of the channel to pinch-off when considering thin oxide capacitance to ground over a gate region. These effects will now be studied in more detail by use of two different shift register bit layouts.

Bit Layout I

In the case of a shift register with two internally generated phases, a major problem is charging and discharging the phases in a short enough time to prevent other major problems. For this reason, the following bit configuration is tried. The schematic is given in Figure 19 and the bit layout is given in Figure 21.

Note that in this configuration the highest voltage level for best discharge should be on the V_{in} line. This fact lessens the restrictions on the $\phi 2$ and the $\phi 4$ generators. C_T represents the total capacitance of all the gates and lines of either $\phi 2$ or $\phi 4$. Since this may be a considerable amount relative to the small capacitance on the gate of the input, $\phi 2$ and $\phi 4$ are constrained to the bottom MOSFET where the voltages may be

less and yet still produce good switching times. This allows the use of smaller MOSFETS in the phase generators than would be possible otherwise. The operation of the bit will now be analyzed for failure modes.

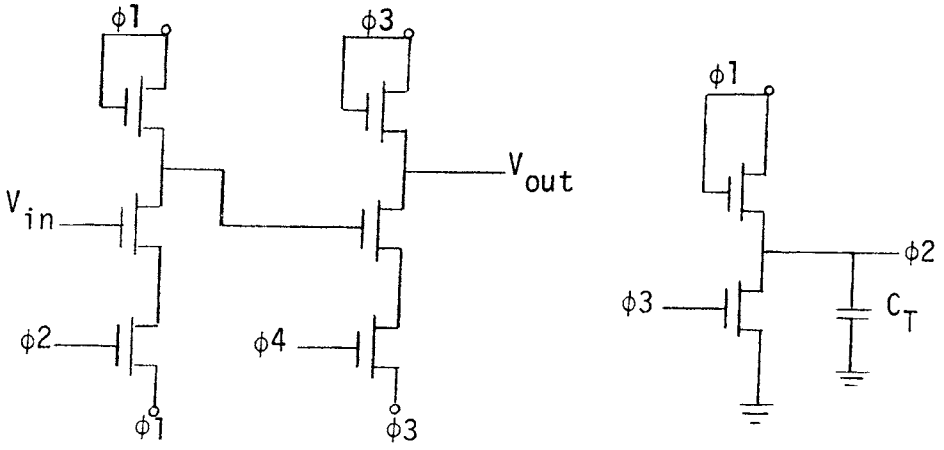


Figure 19

Use the first inverter and its associated capacitance in conjunction with the phase generator φ2. The effect of the phase generator will be on a per inverter basis.

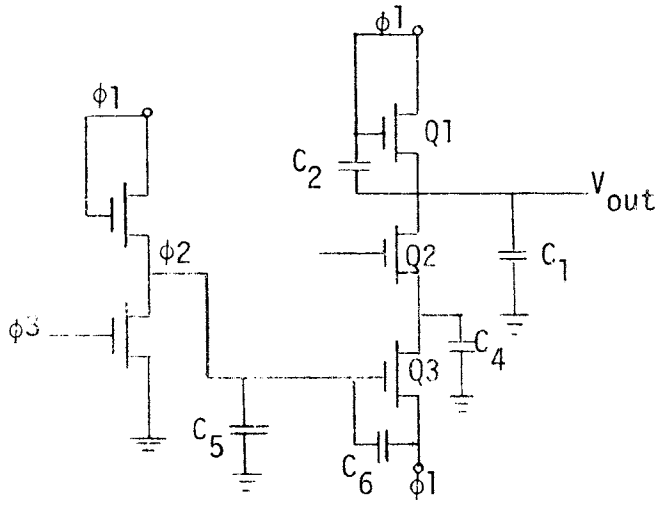


Figure 20
φ2 Generator Driving
Inverter Bit I

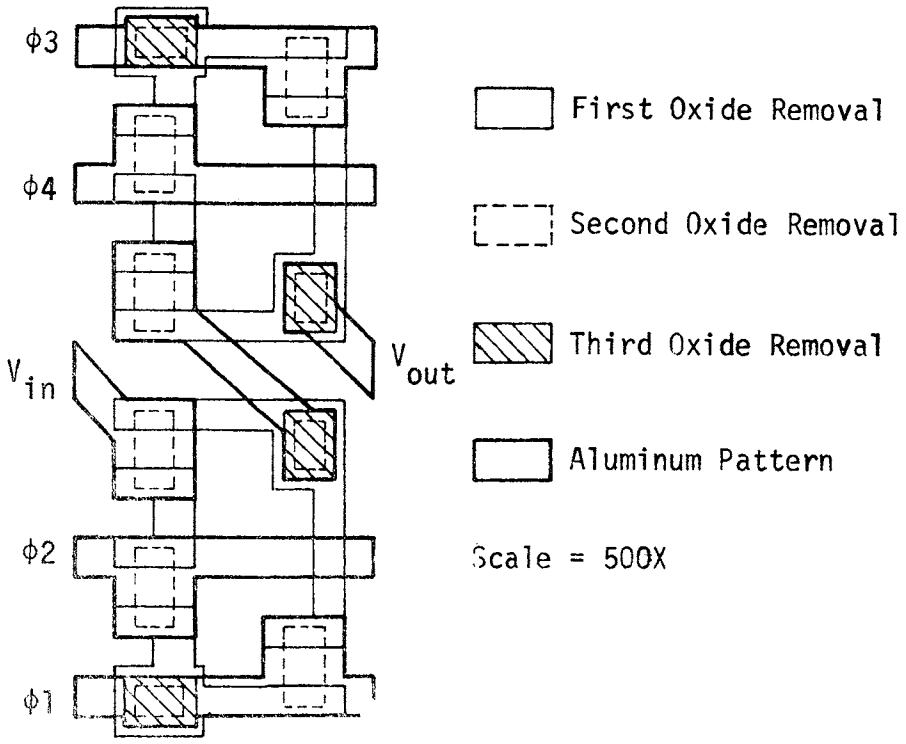


Figure 21

Bit Layout I
4φ Shift Register Bit

$C_1 = (.032\ pf/mil^2)(2.55\ mil^2) = .0815\ pf$

$C_2 = (.3X.4\ mil^2)\ X\ .2\ pf/mil^2 = .024\ pf$

The thin oxide capacitance from gate to source includes only the overlap capacitance since the source is at a 1 level voltage.

$C_4 = (.96\ mil^2)(.05) = .04\ pf$

$C_5 = (3.0X.4)\ X\ .02\ pf/mil^2 = .024\ pf$

$C_6 = (.45\ X\ .4\ mil^2)(.2\ pf/mil^2) = .036\ pf$

This capacitance includes both the overlap and 2/3 of the gate thin oxide capacitance since $\phi 1$ will be ground and is on the source side of Q_3 at the period to be investigated.

Operation:

First assume proper operation with degradation of $\phi 2$ due to coupling between C_5 and C_6.

$$V_{\phi 1} = V_{\phi 3} = -27V \qquad V_{in\ (initial)} = V_{out\ (initial)}$$

V_{out} charges to -20V during $\phi 1$, and $\phi 2$ charges to -20V during $\phi 1$. When $\phi 1$ turns off there will be a +27V signal coupled from the gate to the source of Q_1 through C_2 and from the gate of Q_3 to the source of Q_3 through C_6. The capacitances C_6 and C_5 form a capacitive divider for the signal on $\phi 2$.

$$\phi 2\ (final) = \phi 2\ (initial)\ \frac{C5}{C5+C6} = \frac{-20(.024)}{.060} = -8.0V$$

With -8 volts on the gate of Q_3 the transistor will still be on and capacitor C_4 will discharge to ground, thus leaving the rest of the overlap

capacitance C_7 in parallel with C_6. The output is now,

$$\phi 2 \text{ (final)} = \phi 2 \text{ (initial)} \frac{C5}{C5+C6} - \phi 2 \text{ (initial)} \frac{C7}{C5+C7}$$

$$= -8.0 + \frac{20(.028)}{.052}$$

$$= +2.8 \text{ volts}$$

This analysis shows that there would be a positive voltage on the gate which depends on the MOSFET being turned on. Therefore, the voltage on the gate would stabilize at a level just below turn-off for the MOSFET. This leaves the same voltage across C_4. Since $\phi 2$ is never on after $\phi 1$, the '1' level of the output can never go to zero thus rendering the circuit inoperable.

This type of circuit configuration also contains other problems. Suppose that four external phases were supplied to the circuit thus solving the previous problem. The degradation of the output signal is now considered. The output level is coupled back to $\phi 1$ through C_2. When $\phi 1$ goes off a +27 volt signal is coupled from C_2 to C_1.

$$V_{out \text{ (final)}} = V_{in} \frac{C}{C1+C2} = -20 \frac{.0815}{.1055} = -15.4V$$

Now the input to Q2 will always precharge during the transfer of data from the previous inverter during time. This turns on Q2 and allows the data '1' level to further degrade by charge sharing between C_1 and C_4.

An empirical formula for the p-n junction capacitance is given by,

$$C_{pn} = \frac{.08A}{\sqrt[3]{.6+V_R}} \text{ pf}$$

where C_{pn} is capacitance in picofarads, A is the area of the junction in square mils, and V_R is the reverse bias voltage of the junction.

The equations for capacitances C_1 and C_4 will be used to find the final steady state voltage.

Areas $A_1 = 2.55\ mil^2$ $A_4 = .72\ mil^2$

$$C_1 = \frac{.08A_1}{\sqrt[3]{.6+V}}\ pf \qquad C_4 = \frac{.08A_4}{\sqrt[3]{.6+V}}\ pf$$

$$C_1V + C_4V = Q\ (initial) = \frac{(15.4)(.08X2.55)}{\sqrt[3]{.6+15.4}} = 1.25X10^{-12}\ Coulomb$$

$$V_{(final)}\ \frac{.08A_1}{\sqrt[3]{.6+V_f}} + \frac{.08A_4}{\sqrt[3]{.6+V_f}} = C_1\ V\ (initial)$$

$V_{(final)}$ = 11 volts satisfies this equation. Therefore, V_{in} = -11V. This is a total degradation of 9 volts from the maximum possible. Even if the internal phase generators were made to work, the circuit is still only on the edge of operation. One of the major reasons for this type of circuit configuration was to keep V_{out} at a maximum level. Since this was not the case, the inverted configuration will now be analyzed.

Bit Layout II

The schematic is given in Figure 22 and the layout is given in Figure 23.

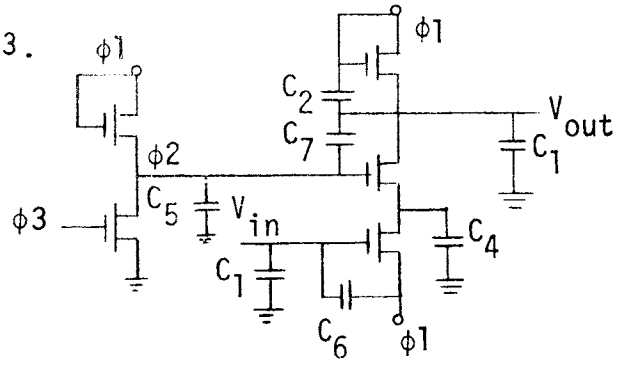


Figure 22

φ2 Generator Driving Bit II Inverter

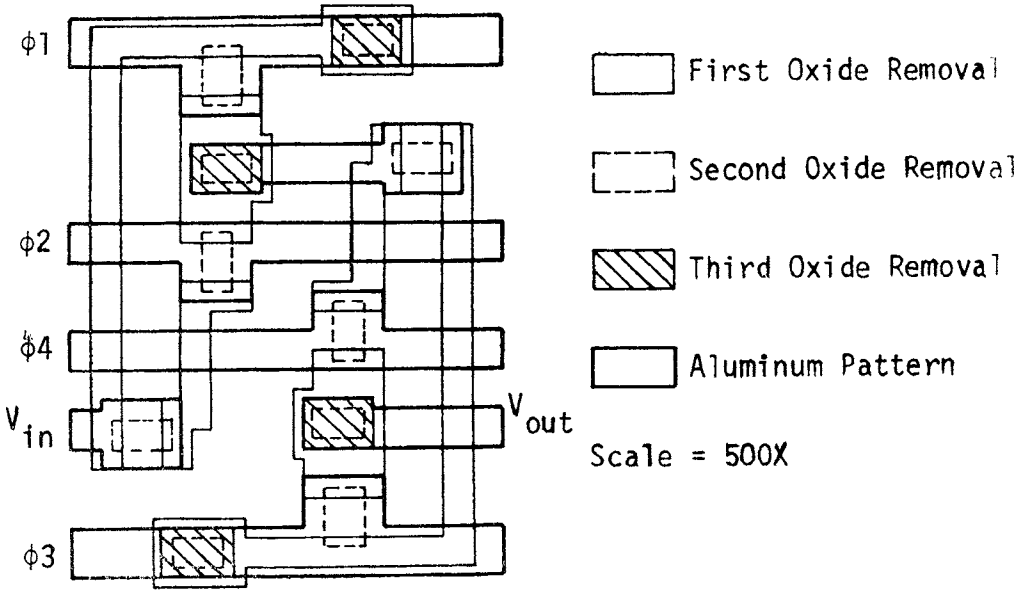


Figure 23
Bit Layout II

C_6 involves only the change in the length of the channel to pinch off under the conditions of $\phi 1$ on, $\phi 1$ off of device Q3.

The output is degraded by $\phi 3$ turning off coupling a positive 27 volt signal through C_6 of the next inverter and also by $\phi 1$ turning off coupling a +27 signal through C_2.

$$V_{inf} = -20 + \frac{27C_2}{C1+C2} = -20 + \frac{27(.024)}{.0763+.024} = -13.7V$$

$$V_{inf} = -13.7 + \frac{27\ C6}{C6+C1} = -13.7 + \frac{27(.006)}{.0823} = -11.7V$$

$\phi 2$ may be degraded by $\phi 1$ turn off through C_2 and C_3 and also by the overlap within the phase generator itself.

.3pf = overlap C in phase generator and crossovers

3.7pf = Total $\phi 2$ capacitance.

For the discharge through C_2, C_7 and C_5 the following equivalent is used.

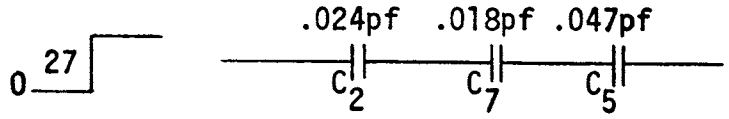


Figure 24 Capacitance Model of Figure 23

$$V_{C5} = \frac{(27)(.01)}{(.01+.047)} = +4.7V$$

$$\phi 2 = -18+4.7 = -13.3V$$

This configuration stabilized at voltages of $V_{\phi 2} = -13.3V$ and $V_{out} = -11.7V$. These are still in the proper order and will enable the circuit to operate. For improved circuit performance, however, the effects of the overlap capacitance must be lessened. The two methods for improving performance are: (1) minimize overlap of the gate over the source, (2) increase the output capacitance of each inverter.

The first solution is the ideal way to go, but practically decreasing the overlap of the gate oxide over the diffusion also decreases the yield per wafer due to alignment problems.

The second solution is the best from a practical production standpoint. The diffusion between the source of the load transistor and the drain of the second transistor may be increased to the point where the effect of the overlap capacitance is reasonable and yet the output is not too loaded to prevent a full charge and discharge. These specifications are determined by the application itself and can be worked out satisfactorily in most instances. Note that this solution has two major drawbacks. The first is that the potential operating speed of the circuit has been slowed down, and the second is that the circuit size may be increased by one-third to one-half.

Circuits involving the two bit-layouts described have been built by Texas Instruments, Inc. of Dallas, Texas. They exhibited characteristics of operation like the calculations show. A third circuit has been developed incorporating the solutions mentioned above and has excellent operating characteristics. It is currently being marketed under the Texas Instruments product number TMS 7D 3300 LA.

Chapter VI

Summary and Conclusions

The first five chapters of this thesis have dealt with the basic background of MOS device construction and operation, the equations and parameters describing the operation, and the methods by which this background can be used in designing a MOSFET digital integrated circuit, especially in the area of 4ϕ logic design. The background presented, although directed toward 4ϕ design is general and may be used with any type of design in the charge and discharge of capacitive loads through MOS devices.

Much of the material was presented in a very general manner either because the inclusion of any more depth would have deterred from the attainment of the 4ϕ objective or because the material may be easily found in one of the references cited. The discussion was intended to be of a practical nature yet reveal state-of-the-art developments in MOS circuit design.

It must be realized that any design or any attempt at optimization of a design depends very strongly on the actual photo-processing of the circuit itself. All processes, though similar, will yield different constants for the equations used in this paper. Therefore, the processing parameters must be well known to give the designer margins within which successful circuits may be realized.

For good designs, one must know both the essential processing parameters and also the transient circuit theory as presented in this paper.

Much work remains to be done in the area of theoretical circuit theory. The optimization of device size with respect to the input gate voltages can be expanded at length to show mathematically a result similar to the empirical result determined in this paper.

Another area to be expanded is the derivation of the exact equations of capacitive discharge through two or more MOSFETS in series. Exactly what occurs during the discharge is obscured by the changing states of the MOSFETS in series. The results of laboratory tests of various combinations of MOSFETS and voltages have been shown in this thesis, but they have not been characterized mathematically.

With the results of this type of analysis computerized design of a more exact nature could be formulated to handle much of the determination of MOSFET sizes. MOS digital logic integrated circuits lend themselves better to complete computerized design than any type of circuitry. The concept of automated layout is now a reality, and with the advent of complete characterization of design equations, computerized design from start to finish might soon become a reality.

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Vita

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He was a graduate assistant at the University of Missouri - Rolla from January 1965, to June, 1967. He has been employed at Texas Instruments, Inc., Dallas, Texas, since June, 1967, where he has done state-of-the-art design and development in MOSFET digital integrated circuits.